Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

1. (Currently amended) A bus interface converter capable of converting an AMBA AHB bus protocol into an i960-like bus protocol, comprising:

an AHB interface for accomplishing interface processing for the AMBA AHB bus protocol;

an i960-like interface for accomplishing interface processing for the i960-like bus protocol; and

a main controller for accomplishing bus protocol conversion between the AHB interface and the i960-like interface;

wherein, the AHB interface comprising:

an AHB bus signal register module for accomplishing judgment and register for control signal from an AMBA AHB bus; and

an AHB bus signal response module for generating corresponding response indicating signal of the AMBA AHB bus protocol;

the i960-like interface comprising:

a bus interface multiplexing request module for generating bus interface multiplexing request signal; and

a bus multiplexing module for accomplishing the multiplexing between an address bus for outputting from an AHB to an i960-like and a data bus for outputting from an AHB to an i960-like;

wherein a clock of the i960-like interface can be set to be in a normal mode or a low-power mode; in the low-power mode, the clock of the i960-like interface is dynamically controlled by the bus interface multiplexing request signal sent by the bus interface multiplexing request module; when there is communication between the AHB bus and an i960-like bus, the clock of the i960-like interface is valid; and when there is no communication between the AHB bus and the i960-like bus, the clock of the i960-like interface is set high to suspend.

2. (Currently amended) The converter according to Claim 1, wherein the AHB bus signal register module further comprises:

an AHB bus write buffer module for performing buffering to ~~the~~ write data and a write address from the AHB bus.

3. (Currently amended) The converter according to Claim 2, wherein the AHB bus write buffer module comprises two buffering fields[[·]] including an address field and a data field.

4. (Currently amended) The converter according to Claim 2, wherein the AHB bus write buffer module has an enabling port, and can set the size of buffering fields for the address field and the data field of the AHB bus write buffer module via the AHB bus.

5. (Currently amended) The converter according to Claim 1, wherein the AHB bus signal response module serves to generate AMBA AHB bus feedback signals including HREADYout and HRESP.

6. (Currently amended) The converter according to Claim 1, wherein the i960-like interface has a request and response function of an accessing outside shared bus, which can be connected to a bus interface multiplexing controller and then connected to the i960-like bus after bus multiplexing.

7. (Currently amended) The converter according to Claim 1, wherein the i960-like interface can be directly connected to the i960-like bus.

8. (Currently amended) The converter according to Claim 1, wherein the bus interface multiplexing request module determines whether to send the bus interface multiplexing request signal to the bus interface unit based on a state indicating signal from the main controller, and determines whether to stop sending the bus interface multiplexing request signal to the bus interface multiplexing controller based on a response signal from the i960-like bus.

9. (Currently amended) The converter according to Claim 1, wherein [[a]] an address and data multiplexing output bus of the bus multiplexing module is connected to a top interconnected logic module, and multiplexed with an ADS-IN signal into a tri-state dual-direction address data bus signal through a tri-state gate.

10. (Previously presented) The converter according to Claim 1, wherein the main controller has two clocks being synchronous with an AHB bus clock and an i960-like bus clock respectively.

11. (Previously presented) The converter according to Claim 1, wherein a clock frequency of the AHB bus may be N times of that of the i960-like bus, where N is a natural number no less than 1.

12. (Previously presented) The converter according to Claim 1, wherein the main controller has a state machine, which serves to indicate the current state of the main controller, and the state machine has three states: idle, read and write.

13. (Canceled)